## AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph [47] beginning on page 11 of the Specification in the Detailed Description with the following corresponding replacement paragraph:

**[47]** Each of 218A and 218C includes a plurality of serial-to-parallel converters 234A-N in sequence, respectively, with registers 236A-N. Each of converters 234 of module 218A is connected to TDM interface logic module 219. Each of converters 234 of module 218C is connected to PAD logic 212. Interface logic modules 218A and 218C convert each of the serialized synchronous data stream from DSO links into a plurality of parallel data units. In the illustrative embodiment, parallel data units are sized as 8-bit bytes, however, other size data units, including 4-bit, 16-bit, or 32-bit, etc., data units may be similarly utilized. Registers 236A-N are coupled to a multiplexer 238. The output of multiplexer 238 ~~servers~~ serves as the output of TDM Interface logic module 218 and is coupled to SAL logic 220.

Please replace Paragraph [65] beginning on page 19 of the Specification in the Detailed Description with the following corresponding replacement paragraph:

**[65]** As illustrated in Fig. 4, each TDM logic 218B and 218D includes a plurality of registers 236A-N in sequence, respectively, with parallel-to-serial converters ~~235A-N~~ 234A-N. Each sequential pair of registers 236 and converters 234 of TDM logic 218B is connected TDM logic 219. TDM logic 218B converts each of the parallel data units or bytes from egress memory 260 into a serialized synchronous data stream which is supplied to data framers TDM logic 219. Each sequential pair of registers 236 and converters 234 of TDM logic 218D is connected PAD logic 212. TDM logic 218D converts each of the parallel data units or bytes from egress memory 260 into a serialized synchronous data stream which is supplied to the DSP in PAD logic 212 for further forwarding.